Docket No.: S3-02P16504

CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of the amended claims attached to the International Preliminary Examination Report issued by the International Preliminary Examination Authority for International Patent Application PCT/DE2003/003090 on April 1, 2005.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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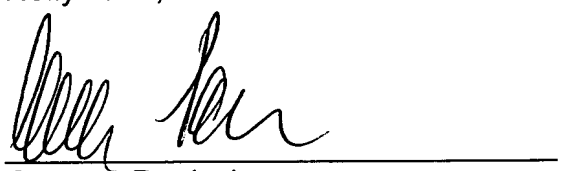

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Description

Method and device for actuating a power switch

The invention relates to a method for actuating a power switch according to the preamble of Claim 1, in particular a semiconductor power switch arranged between two energy storage devices in a wiring system of the vehicle equipped with an integrated starter generator. It also relates to a device for implementing said method according to Claim 2.

In a wiring system of the vehicle with ISG, switching processes are necessary between the energy storage devices - accumulators of different nominal voltages and capacitors (intermediate circuit capacitors, double layer capacitors) - via static frequency changers or switching regulators by means of power switchs which are carried out on the commands of a control unit.

A requirement in this case is that before a switch is opened, the switch current flowing through it is brought to 0A and that before a switch is closed, the switch voltage between its switching contacts is brought to 0V so that the switch can be actuated in a zero-power state.

A switch current 0A can be implemented, for example, by disabling an AC/DC static frequency changer or a DC/DC switching regulator and causes no problem in practice.

Regulation to the 0V switch voltage, i.e. no potential difference between the poles of the (opened = non-conductive) switch, usually takes place by deliberately reversing the charge of one of the energy storage devices, for example, an intermediate circuit capacitor, since this is usually the smaller of the energy storage devices. In principle, this regulation can also be carried out by means of a static

frequency changer or a switching regulator positioned between said static frequency changer and the wiring system of the vehicle.

The intermediate circuit capacitor for example has a capacity of several 10.000μF, the double layer capacitor for example a capacity of 200F and the accumulators a capacity of several Ah. The switch voltage to be equalized can be up to a voltage of 60V.

However, determined by the unfavorable ratio of the power of the static frequency changer (e.g. 6kW) or the switching regulator (e.g. 1kW) to the energy required for charge equalizing (up to 40 joules), stringent limits have also been set in practice for voltage equalizing.

If now for example, for reasons of reliability and space requirements, semiconductor switches are used as switches, the accuracy of voltage equalizing which can be achieved in this way is not sufficient.

Currents and powers occurring during normal operation require the use of components (capacitors, switches) with very low resistances. In the case of existing voltage differences, the equalizing currents are accordingly high across the switch to be closed. In extreme cases, this leads to a destruction of the semiconductor.

A limitation of the equalizing current flowing through the switch to a safe value requires a current measurement which necessitates a cost-intensive current sensor at the peak of the occurring currents. In addition, the equalizing process cannot be carried out time-optimized because in the case of an excessive switch voltage, the power loss in the switch is high which represents a further possible limitation.

The object of the invention is to create a method and a corresponding device for actuating a semiconductor power switch which functions without a cost-intensive current sensor and in the case of which the transient effect and the closed circuit condition are controlled in such a way that, even in the case of a high voltage difference at the switch, damage to the semiconductor is excluded.

This object is achieved according to the invention by means of a method in accordance with the features of Claim 1 and a device in accordance with the features of Claim 2.

A method and a device for switching a semiconductor power switch are proposed in which the outstanding feature is that the resistance of the switching path of the semiconductor power switch is controlled so that the chip temperature of the semiconductor power switch does not exceed a predetermined nominal temperature, in this case, when the predetermined nominal temperature is reached, the resistance of the switching path of the semiconductor power switch is increased, which on the one hand causes the power dissipation to fall and on the other hand lowers the chip temperature as a result of the reduced power dissipation.

Advantageous further developments of the invention can be taken from the subclaims.

The inventive method includes the technical theory to control the resistance of the switching path of the semiconductor power switch by a control voltage so that the temperature in the power switch (chip temperature) does not exceed a predetermined value or is held at a constant value, with the control variable acting as a control signal for generating the control voltage.

With an arrangement for executing this method, provision is made for embodying the switch as a transfer gate with special semiconductor transistors into which diodes for recording the chip temperature are integrated, and for controlling it in such a way by means of a charge pump, that the chip temperature of the transistors is regulated and can be limited to a predetermined nominal value.

Advantageously the predetermined nominal temperature lies in the operating range of the power semiconductor. On the one hand this prevents the power switch being operated above its permitted temperature and on the other hand, because it is operated in this way, prevents the lifetime of the power semiconductor being reduced.

Advantageous further developments of the invention can be taken from the subclaims.

An embodiment of the invention is explained below in greater detail on the basis of a schematic drawing. The drawings show:
Figure 1 a basic circuit diagram of a 14V/42V wiring system of a vehicle,
Figure 2 a basic circuit diagram of a semiconductor power switch embodied as a transfer gate,
Figure 3 the circuit of a transfer gate which can be controlled by means of a charge pump,
Figure 4 a temperature recording device with nominal value comparison and logic gates.

Figure 1 shows a basic circuit diagram of a 14V/42V wiring system of a vehicle with an integrated starter generator ISG connected to an internal combustion engine (not shown) on the basis of which the invention is explained in greater detail.

This ISG is connected by means of a bidirectional AC/DC

converter AC/DC

a) directly to an intermediate circuit capacitor C1,

b) via a power switch S2 to a double layer capacitor DLC,

c) via a power switch S1 to a 36V accumulator B36 and a 42V wiring system of a vehicle, and

d) via a bidirectional DC/DC converter DC/DC to a 12V accumulator B12 and a 14V wiring system of a vehicle N14.

According to the invention, in accordance with a program which is not explained in further detail, each power switch (S1 and S2) should be embodied as a transfer gate which is controlled by a charge pump actuated by the commands from a control unit which is not shown.

Figure 2 is a basic circuit diagram of a switch embodied as a transfer gate TG, for example, for the switch S2 which is arranged between the intermediate circuit capacitor C1 and the double layer capacitor DLC. If further switches other than the switches embodied as a transfer gate are required, these are embodied identically.

The transfer gate TG consists of two MOSFET transistors Q1 and Q2 connected in series whose source connections s and gate connections g are interconnected in each case. The drain connections d serve as input E or output A of the switch.

Because in the wiring system of a vehicle, the voltage differences Vdiff and the current directions at the switch can have any leading sign or any direction, two transistors or groups of transistors connected in series must be used, of which at least one of them is blocked in each case in the blocked state of the power switch. Such an arrangement is known as the transfer gate which performs the actual switching function.

Such a switch embodied as a transfer gate is controlled by

applying a control voltage between the source connection and the gate connection. In order to reduce the control voltage, a resistor not described in greater detail in this case is provided between the gate and the source connection.

There is provision in accordance with the invention, as indicated in Figure 2, for using commercially-available transistors with integrated temperature sensors (D1A, D1B, D2A and D2b) in the transfer gate as semiconductors Q1 and Q2, which are known for example from the "Philips Semiconductors Product Specification, Power MOS transistor voltage clamped logic level FET with temperature sensing diodes, BUK9120-48TC, February 1998*. On the manufacturer side two antiparallel diodes are integrated to record the chip temperatures for each PowerMOSFET, however in the exemplary embodiment in accordance with the invention only one diode is used per PowerMOSFET Q1, Q2.

In Figure 3, the circuit of switch S2 embodied as a transfer gate which can be controlled by a charge pump, said circuit being arranged between the intermediate circuit capacitor C1 and the double layer capacitor DLC, is shown once more, but without the integrated temperature sensor. In addition, it is possible that by means of a signal Dis via a further transistor Q3 arranged in the transfer gate (and an external transistor Q4), the control voltage can be short-circuited in order to open the transfer gate quickly (to make it non-conductive).

The charge pump LP known per se (capacitors C2 to C5 and diodes D3 to D5) sets up a control voltage between the source connection and the gate connection s, g of the transfer gate (switch 2). It is supplied by a gate oscillator (logical circuit elements U1 up to U4) having an enable function. In this way, both the oscillator and the charge pump LP can be

enabled and disabled by a logical control signal En (enable). The generation of this control signal En is explained further below.

By enabling the charge pump LP by means of a signal En (enable), a positive control voltage is set up between the source connection and the gate connection as a result of which switch S2 (transfer gate) accordingly becomes conductive. After the disabling process, this voltage is again reduced as a result of which switch S2 again becomes non-conductive. The enabling and disabling takes place controlled in time, i.e. by means of explicitly enabling and disabling the charge pump, the transfer gate can be kept in an similar conductive state.

Figure 4 shows the inventive circuit for recording the chip temperatures of transistors Q1 and Q2 of the transfer gate TG with nominal comparison and logical signal combination.

This temperature recording unit consists for each transistor Q1, Q2, of a series circuit at the poles of a voltage source (which can be an existing 5V supply), consisting of a resistor R7, R8 and the temperature-sensitive diode DT1, DT2 (which corresponds to the diode D1B, D2B in Figure 2), which causes a working current of 1mA to flow through the diodes DT1, DT2.

The connection point between resistor R7 and diode DT1, or resistor R8 and diode DT2, is linked in each case to the non-inverting input of a comparator K1 or K2, at the inverting input of which lies a nominal voltage VTsoll assigned to a nominal temperature Tsoll. The outputs of the two comparators K1, K2 are connected to the inputs of a first logic element NAND, of which the output is connected to the input of a second logic element NOR, to the other input of which an ON/OFF signal is fed, which will be discussed in more detail below. The enable signal En, which is fed to the gate

oscillator of the charge pump. appears at the output of the second logic element NOR. The diodes DT1, DT2 for recording the chip temperatures have a negative temperature coefficient, i.e. as the chip temperature increases the flux voltage reduces monotonously at around 1.6mV/°C. The value of the flux voltage at 25°C is 660mV for example.

As a result of the structure of the transfer gate one transistor is operated with reverse polarity in each case (drain-source voltage), whereas the other carries the major part of the switch voltage. The chip temperatures also develop in a correspondingly different way during the switch-on process. It is thus necessary to record the temperatures of the transistors Q1, Q2 separately and to align the regulation to the higher temperature in each case.

The following information can be taken from the tables shown below (in which high = H and low = L; an underscored reference signal means that the signal at its output is meant):

	A			B			C		
	K1	K2		K1	K2	NAND	NAND	ON/OFF ON = L OFF=H *Dis*	NOR *En*
VT1ist>VTsoll	H	-	→	L	L	H	→ L	L	H
VT1ist<VTsoll	L	-		L	H	H	H	L	L
VT2ist>VTsoll	-	H		H	L	H	L	H	L
VT2ist<VTsoll	-	L		H	H	L	H	H	L

Table A: Provided the diode voltage VT1ist, VT2ist generated by the relevant chip temperature T1ist, T2ist is greater than a predetermined nominal voltage value VTsoll assigned to an

increased but permitted chip temperature Tsoll, the output of the assigned comparator K1, K2 is at a high signal.

Table B: As soon as the diode voltage VT1ist, VT2ist assigned to the relevant chip temperature T1ist, T2ist falls below the predetermined nominal voltage value VTsoll, the output of the assigned comparator K1, K2 goes to a low signal and the output signal of the first logic element NAND jumps to a high signal.

Table C: If the output signal of the first logic element NAND goes to a high signal, the output signal of the second logic element NOR which follows it (enable signal En) jumps to a low signal, whereby the charge pump LP stops and the transfer gate becomes non-conducting.

An ON/OFF signal can be taken from Figure 4 and Table C. This already mentioned signal is a command of the control device which is not shown in the Figure. It is always ON = low if the associated switch S1, S2 is to be conducting and is OFF = high if this switch is to be non-conducting.

This ON/OFF signal is identical to the signal Dis in Figure 3, which rapidly makes the switch S1, S2 non-conducting by short-circuiting the gate-source path and holds it in this state for as long as OFF = high.

It can also be seen from Table C that the charge pump LP can only make the switch conducting if on the one hand the control device for it gives its permission (ON = Dis = low) and if on the other hand the output signal of the first logic element NAND signals by its low state that no chip temperature has exceeded the nominal value. The output signal En of the second logic element NOR then goes to a high level and the subsequent gate oscillator (U1 to U4, Figure 3) creates a rising gate voltage for the transfer gate Q1, Q2 which conducts noticeably

more strongly. The current through Q1, Q2 thereby increases and thus the power dissipation and the chip temperature as well, at which point the flux voltage of the temperature-sensitive diodes DT1 and DT2 falls. This goes on until the VT1ist or VT2ist falls below the value VTsoll. Enable signal En goes to low and the oscillator stops. The charge pump LP no longer delivers any gate voltage = control voltage Vst and capacitor C1 discharges itself through resistor R1, which causes the gate voltage to fall slowly. The transfer gate becomes more non-conductive, the power dissipations of the transistors Q1 and Q2 fall and thereby also the chip temperatures, at which point the flux voltages of the diodes DT1 and DT2 rise again and the process starts over.

Overall this produces a two-state controller of which the oscillator frequency and amplitude depend on the delay times of the control elements.

Patent claims

1. Method for switching a semiconductor power switch (S1, S2), characterized in that
the resistance of the switching path (E-A) of the semiconductor power switch (S1, S2) is controlled via a control input (s, g) by a control voltage (Vst) and/or a control current depending on the chip temperature (T1ist, T2ist) to such an extent that the chip temperature (T1ist, T2ist) of the power switch (S1, S2) does not exceed a predetermined nominal temperature Tsoll, in which case, when the nominal temperature (Tsoll) is reached, the resistance of the switching path (E-A) is increased.

2. Device for implementing the method according to Claim 1, especially for actuating a semiconductor power switch (S1, S2) arranged between two energy storage devices (C1, DLC, B36) in a wiring system of the vehicle equipped with an integrated starter generator(ISG),
characterized in that
the power switch (S1, S2) which can be controlled by means of a control voltage Vst so that it conducts or does not conduct is embodied as a transfer gate (TG)
- which features two transistors (Q1, Q2) or groups of transistors connected in series of which, in the off-state of the power switch (S1, S2), at least one is blocked, and
- in which each transistor (Q1, Q2) or each group of transistors is assigned at least one diode (DT1, DT2) for recording the chip temperature (T1ist, T2ist),

for generating the control voltage (Vst), a charge pump (LP) is provided by means of which the transistors (Q1, Q2) of the power switch (S1, S2), in the conductive state, are in each case only controlled to such an extent that the chip

temperature (T1ist, T2ist) of each transistor (Q1, Q2) of the power switch (S1, S2) does not exceed a predetermined required temperature Tsoll, and
a temperature recording unit is provided in which the comparison of the chip temperatures with the required value is undertaken, and which delivers an enable signal (En) assigned to this comparison for the charge pump (LP), with the resistance of the switching path (E-A) being increased when the required temperature is reached.

3. Device according to claim 2, characterized in that a transistor (Q3) is assigned to the transfer gate (S1, S2, TG), of which the collector-emitter path is arranged between the interconnected gate connections (g) and the interconnected source connections (s) of two transistors (Q1, Q2) or groups of transistors connected in series, and
which can be shifted by means of an external signal (Dis) to the conductive state in order to rapidly make the transfer gate (TG) non-conductive.

4. Device according to claim 2 or 3, characterized in that the temperature recording unit features at least one series circuit at the poles (+5v, GND) of a voltage source, consisting of the diode (DT1, DT2) assigned to it and a resistor (R7, R8) for each transistor (Q1, Q2) or for each group of transistors,
the connection point between resistor (R7, R8) and diode (DT1, DT2) at which a voltage (VT1ist, VT2ist) assigned to the chip temperature (T1ist, T2ist) can be tapped, is connected in each case to the input of a comparator (K1, K2),
at another input of the comparator (K1, K2) a nominal voltage (Vtsoll) assigned to the predetermined nominal temperature (Tsoll) is applied,
the comparator (K1, K2) performs the comparison of the voltage

(VT1ist, VT2ist) assigned to the chip temperature (T1ist, T2ist) with the nominal voltage (VTsoll) assigned to the predetermined nominal temperature (Tsoll),
the outputs of all comparators (K1, K2) are connected to the inputs of a first logic element (NAND),
the output of the first logic element (NAND) is connected to the input of a second logic element (NOR) of which an ON/OFF signal (Dis) is fed to the other input, and
the output signal of the second logic element (NOR) is fed to the gate oscillator (U1 to U4) of the charge pump (LP) as an enable signal (En).